

APPLICANT(S): Iny, Ofer  
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FILED: June 1, 2001  
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### **REMARKS**

The present Response is intended to be fully responsive to all points of rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application are respectfully requested.

### **Status of Claims**

Claims 8-33 are pending in the application.

Claims 1-7 have been canceled without prejudice or disclaimer. In making this cancellation without prejudice, Applicant reserves all rights in these claims to file continuation or divisional patent applications.

New claims 8-33 have been added.

No new matter has been added.

### **OBJECTIONS TO DRAWINGS**

The Examiner objected to the drawings, because in Fig. 4, the labels for Queue Tail 0 (115) and Queue Head 0 (117) appear to be switched from where the specification says they are supposed to be on page 5.

Amended Figs. 4-6 include the queue tail and queue head labels in compliance with the description in the specification.

Accordingly, applicant requests the objection to the drawings be removed.

### **Amendments to the drawings**

In Figs. 5 and 6, the reference number of the labels "Global delete pointer", and "Global write pointer" were amended to be consistent with the specification.

In Fig. 7 the notations relating to the "head", and "tail" memories were amended to be consistent with the specification, and with the data memory table illustrated in Fig. 7.

These amendments are editorial in nature and add no new matter.

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## **CLAIM REJECTIONS**

### **Claim Rejections under 35 USC §112**

Claim 4 was rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 5-7 were rejected as being dependent upon rejected claim 4.

As claims 4-7 have been cancelled without prejudice, these rejections are now moot.

### **35 U.S.C. § 102 Rejections**

Claim 1 has been rejected under 35 USC §102(b) as being anticipated by Fishler et al. (US Patent No. 5,954,794).

As claim 1 has been cancelled without prejudice, this rejection is now moot.

### **35 U.S.C. § 103 Rejections**

Claim 2 was rejected under 35 U.S.C. 103§(a) as being unpatentable over Fishler et al. in view of Gallup et al. (U.S. Patent No. 5537562).

Claim 3 was rejected under 35 U.S.C. 103§(a) as being unpatentable over Fishler et al. in view of Lauffenburger et al. (U.S. Patent No. 6813249).

As claims 2 and 3 have been cancelled without prejudice, these rejections are now moot.

## **REMARKS TO NEW CLAIMS**

As required by 37 CFR 1.111(c), the following remarks clearly point out the patentable novelty which Applicant thinks the newly added claims 8-33 present in view of the state of the art disclosed by the references cited.

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Newly added independent claims 8 and 21 each include the feature of sequentially inserting a plurality of packets into a circular first-in-first-out memory scheme; and selectively associating the packets with a plurality of queues.

Applicant respectfully asserts that none of the cited references, including Fishler et al., Gallup et al., and Lauffenburger et al., teaches or fairly suggests sequentially inserting a plurality of packets into a circular first-in-first-out memory scheme; and selectively associating the packets with a plurality of queues.

Furthermore, it is respectfully asserted that the distinguishing features of independent claims 8 and 21, as discussed above, would not have been obvious at the time the invention was made to a person skilled in the art, in view of the cited references, alone or in any combination thereof.

In addition, Applicant would like to point out that the features of newly added claims 8 and 21, are supported by the originally filed disclosure. Specifically, Figs. 3-6 and the corresponding description of Figs. 3-6 in the specification, as originally filed, disclose sequentially inserting a plurality of packets into a circular first-in-first out memory scheme. Specifically, as clearly illustrated by Figs. 3-6, the global delete pointer and the write pointer are advanced to through the memory scheme such that each of the pointers initially points to a first memory word, is advanced through consecutive memory words until it reaches the end of the memory, and is then advanced back to the first memory word.

Therefore, newly added independent claims 8 and 21 are patentable, and thus allowable, over the prior art references on record and any combination thereof.

Claims 9-20 are each dependent, directly or indirectly, from independent claim 8 and incorporate all the elements of this claim.

Claims 22-33 are each dependent, directly or indirectly, from independent claim 21 and incorporate all the elements of this claim.

Therefore, it is respectfully submitted that claims 9-20 and 22-33 are patentable, and thus allowable, at least for the reasons set forth above.

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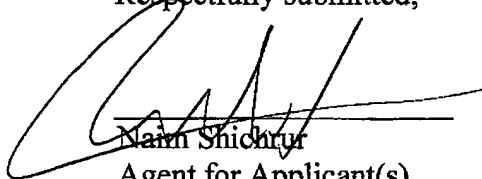
### Conclusion

In view of the foregoing amendments and remarks, the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 50-3355.

Respectfully submitted,



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Dated: March 23, 2005

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### AMENDMENTS TO THE DRAWINGS

The attached sheets of drawings include changes to Figs. 4-7. These sheets replace the original sheets including Figs. 3-7.

In Figs. 4-6, the locations of the labels "queue head 0", "queue tail 0", "queue head 1", and "queue tail 1" have been changed to be consistent with the specification.

In Figures 5 and 6, the reference number of the label "Global delete pointer" was amended to read "114" instead of "112", and the reference number of the label "Global write pointer" was amended to read "112" instead of "114", in order to be consistent with the specification.

Figure 7 was amended to be consistent the specification, and with the data memory table illustrated in Fig. 7. Specifically, the notations "Head Memory", "Head 0=5", "Head 1=9" and "Head n=x", were replaced by "Tail Memory", "Tail 0=9", "Tail 1=5", and "Tail n=x", respectively; and the notations "Tail Memory (pointer, size)", "Tail 0=1 3", "Tail 1=3 2", and "Tail n=x", were replaced by "Head Memory (pointer, size)", "Head 0=0,3", "Head 1=3,2", and "Head n=a,b", respectively.

The above changes are editorial in nature and add no new matter.

Applicants note that formal drawings will be required when the application is allowed.

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Attachment: Replacement Sheets